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Applicant's representative acknowledges with gratitude the courtesies extended by the Examiner during the personal interview of September 4, 2002. The present Preliminary Amendment incorporates the proposed claim amendments discussed in the interview.

Claims 1, 3-11, 25, 27-32, and 39 are now pending in the present application. Claims 1, 11, and 25 have been amended by the present Preliminary Amendment. A marked-up version of these claims, showing changes made, is attached hereto as Appendix A.

Each of the aforementioned claims has been amended to further define the structure. Claim 1 defines, *inter alia*, an “etched via being wider in diameter than said conductive plug.” Claims 11 and 25 define, *inter alia*, a “first etched via [that] is wider in diameter than said conductive plug.” Support for these new claims can be found in Applicant's specification at, for example, Figs. 4 and 5. Claims 1, 3-11, 25, 27-32, and 39 distinguish over the references Chiang and Matsuura applied in the Office Action of April 30, 2002. Neither reference teaches or suggests an etched via that is wider than the conductive plug, as claimed.

Further, as asserted in Applicant's response of July 30, 2002, Chiang teaches that “[t]he aluminum interconnects are not encapsulated because aluminum does not diffuse into silicon dioxide as opposed to copper.” (emphasis added) (Col. 11, lines 40-48). The tungsten plug itself in Figure 11 acts as a diffusion barrier between the aluminum interconnect and the doped region. A second conductor layer is not taught or suggested in the embodiment depicted by Chiang's Fig. 11. In addition, Chiang merely suggests that “the copper within the interconnects is encapsulated to prevent copper diffusion into a silicon dioxide layer.” (emphasis added) (Col. 10, lines 9-11), not to serve as a second conductor layer. Still further, Chiang teaches that Fig. 11 illustrates that “metals other

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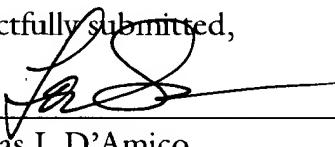
than copper can be used to form interconnects." (Col. 11, lines 12-14) (emphasis added).

Thus, Applicant still maintains that the aluminum of Fig. 11 would not be substituted with a copper/barrier layer of Fig. 9, since Chiang specifically teaches that Fig. 11 illustrates a structure containing metals other than copper to form the interconnects. Accordingly, Chiang fails to teach or suggest the present invention as recited in claims 1, 3-11, 25, 27-32, and 39.

Favorable action is respectfully solicited.

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Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

DICKSTEIN SHAPIRO MORIN &  
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorney for Applicants

**APPENDIX A**

**In the Claims:**

Please amend the claims as follows.

1. (Twice Amended) A semiconductor device comprising:

an insulator layer;

a conductive plug positioned within said insulator layer and formed of a

single conductive material;

a doped region connected to said conductive plug;

an etch-stop layer located on said insulator layer and surrounding said plug;

a non-conductive layer having an etched via at least partially over said conductive plug, wherein said etched via is wider in diameter than said conductive plug; and

a conductive connector formed in said via in electrical contact with said plug and including a first conductive layer deposited in and in contact with said etched via and a second conductive layer deposited over and in contact with said first conductive layer, said first conductive layer including a portion in contact with said conductive plug.

11. (Three Times Amended) A semiconductor device comprising:

at least one memory cell comprising:

an active region in a substrate;

a conductive plug formed of a single conductive material positioned within an insulator layer and provided over said active region, said conductive plug being electrically connected with said active region;

an etch-stop layer deposited on said insulator and around said conductive plug;

an intermediate non-conductive layer provided over said etch stop layer and having at least a first and a second etched via over said plug, said first etched via being wider in diameter than said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a first conductive layer deposited in and in contact with said first and second vias, said first conductive layer including a portion in contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.

25. (Three Times Amended) A processor-based system comprising:

a processing unit;  
a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

a conductive plug formed of a single conductive material positioned within an insulator and provided on a connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via over said conductive plug, said first etched via being wider in diameter than said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said first and second etched vias, said first conductive layer including a portion in contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.